THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

This opinion (1) was not written for publication and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WILLIAM K. BODIN and DALE R. WHITFIELD

Appeal No. 95-4172
Application 08/040,698[1]

ON BRIEF

Before THOMAS, LEE, and TORCZON, Administrative Patent Judges.

TORCZON, Administrative Patent Judge.

DECISION ON APPEAL

BACKGROUND

This is an appeal under 35 U.S.C. § 134 from the final rejection of claims 1-3 and 8, the only pending claims. We reverse.

The subject matter of the invention is a system and method for simultaneous high-resolution display for multiple virtual applications. Claim 8 is representative of the claims on appeal, which stand or fall together (emphasis added):

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[1] Attorney docket no. BC9-93-008.

8. A method for simultaneous high resolution display within multiple applications in a data processing system having a processor, a memory coupled to said processor, a display device coupled to said memory and said processor and a display adapter coupled to said display device and said processor which includes a physical video buffer said method comprising the steps of:

providing a logical video buffer within said memory, said logical video buffer including a bank management function for receiving a multibank high resolution graphic display output which includes both bank and video data from one of a plurality of applications within said data processing system;

detecting an attempt by said one of said plurality of applications within said data processing system to output a multibank high resolution graphic display to said physical video buffer within said display adapter;

writing said multibank high resolution graphic display output from said one of said plurality of applications within said data processing system to said logical video buffer; and

subsequently writing said logical video buffer to said physical video buffer in response to a transition of said one of said plurality of applications from a background task to a foreground task.

The examiner rejected all of the claims under 35 U.S.C. § 103 in view of the following references:

Schumacher	4,567,515	28 Jan. 1986
Agarwal	4,688,167	18 Aug. 1987

Agarwal discloses the claimed hardware and the buffers for handling multiple application displays as virtual displays

in memory. The examiner concedes, however, that Agarwal does not teach the multibanking limitation of the claims.

According to the examiner, Schumacher teaches multibank high resolution displays, apparently with reference to bit planes DØ and D1. (Paper 14 at 4.)

DISCUSSION

The rejection falters on the grounds of claim interpretation. Appellants argue that their claims are governed by 35 U.S.C. § 112[6]. The examiner responds that

> the specification does not mention a multibank high resolution [display] including both multiple banks and multiple planes as Appellant[s] argu[e]. One of ordinary skill in the art can interpret[] the term "bank" as a location for storing information, not necessarily including multiple banks and multiple planes.

(Paper 14 at 6.) Even if this were true, it would be the basis for an indefiniteness rejection, In re Dossel, 115 F.3d 942, 946, 42 USPQ2d 1881, 1885 (Fed. Cir. 1997), which should not be confused with an obviousness rejection. Indefiniteness is not a license to ignore a limitation. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). In any case, the specification states,

> that high resolution graphics displays require multiple banks of memory to be utilized and it is an important feature of the present invention that a logical video buffer is provided which includes multibank management capability.

(Paper 1 at 15.) Appellants provided credible evidence that bank management and multiple banks would have specific meanings to those skilled in the art. (Paper 7 attachment: Richard F. Ferraro, Programmer's Guide to the EGA and VGA Cards 653-656 (2d ed.)[2].)

The examiner's combination of references does not suggest Appellants' method of multibanking with a logical buffer. Unfortunately, neither the examiner nor Appellants explored the range of equivalents to the disclosed structures and acts corresponding to the means and steps in the claims. The record also contains no analysis about the level of skill in the art, the practice of providing logical buffers to expand available memory, or how one skilled in the art might implement a logically buffered multibanking function. Consequently, we have no basis for affirming the examiner's rejection of the appealed claims.

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[2] Although no date is listed, the examiner has not objected to this evidence and the subject matter suggests that it is at least contemporaneous with, if not earlier than, Appellants' filing date.

DECISION

On the basis of the record before us, the rejection of claims 1-3 and 8 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)
JAMESON LEE Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
RICHARD TORCZON Administrative Patent Judge	)

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